DATA SHEET

TDA9851
I²C-bus controlled economic BTSC stereo decoder

Product specification
File under Integrated Circuits, IC02

1997 Nov 12

Philips
Semiconductors

PHILIPS

I²C-bus controlled economic BTSC stereo decoder

TDA9851

FEATURES

- Voltage Controlled Amplifier (VCA) noise reduction circuit
- Stereo or mono selectable at the AF outputs
- Stereo pilot PLL circuit with ceramic resonator
- Automatic pilot cancellation
- Automatic Volume Level (AVL) control (+6 to –15 dB)
- I²C-bus transceiver.

GENERAL DESCRIPTION

The TDA9851 is a bipolar-integrated BTSC stereo decoder for application in TV sets, VCRs and multimedia PCs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8	9	9.5	V
I_{CC}	supply current		–	30	40	mA
$V_{o(rms)}$	output voltage (RMS value)	composite input voltage 250 mV (RMS) for 100% modulation L + R (25 kHz deviation); f_{mod} = 300 Hz	–	500	–	mV
$\alpha_{csL,R}$	stereo channel separation L and R	14% modulation; f_L = 300 Hz; f_R = 3 kHz	–	20	–	dB
$THD_{L,R}$	total harmonic distortion L and R	100% modulation L or R; f_{mod} = 1 kHz	–	0.2	1.0	%
S/N	signal-to-noise ratio	mono mode; referenced to 500 mV output signal				
		CCIR 468-2 weighted; quasi peak	50	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9851	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
TDA9851T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

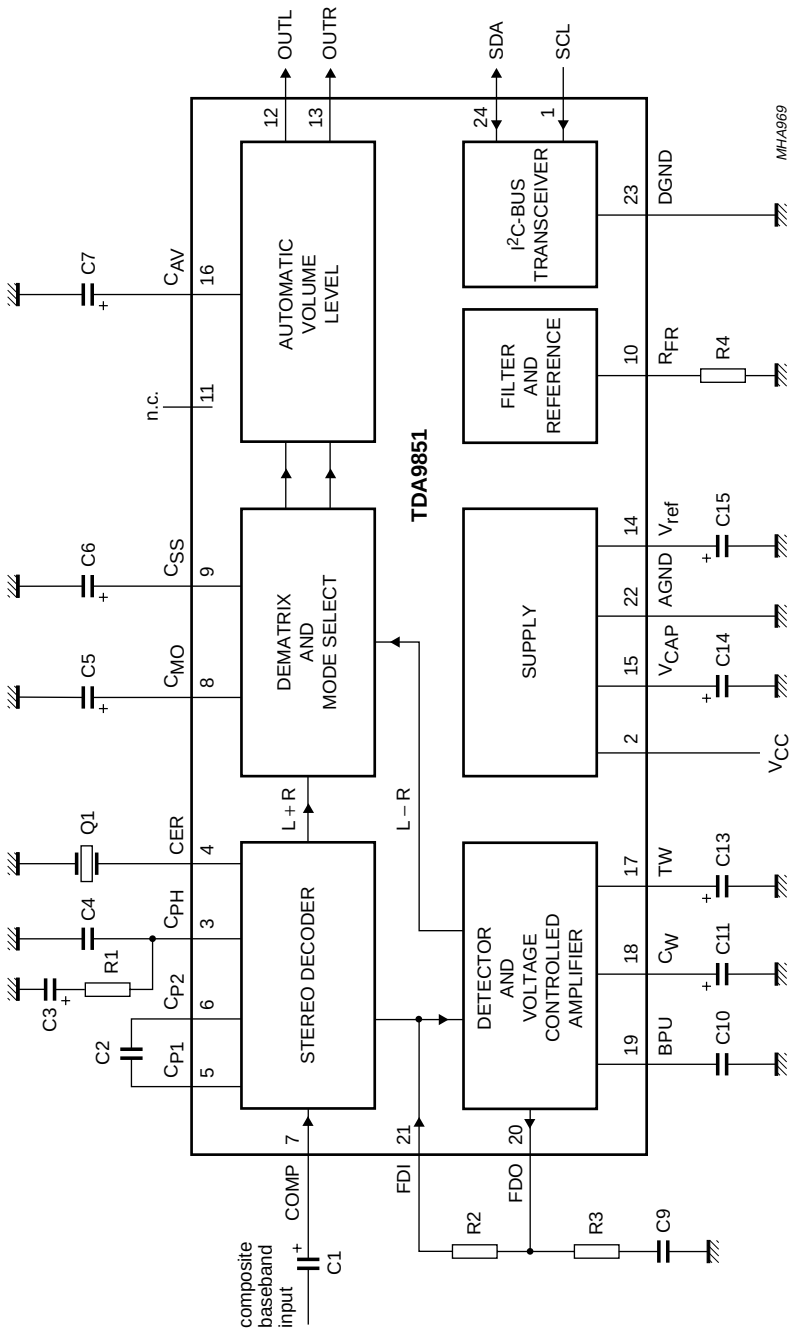


Fig.1 Block diagram.

Component list

Electrolytic capacitors ±20%; foil capacitors ±10%; resistors ±5%; unless otherwise specified; see Fig.1.

COMPONENT	VALUE	TYPE	REMARK
C1	2.2 μF	electrolytic	63 V
C2	220 nF	foil	
C3	2.2 μF	electrolytic	63 V
C4	220 nF	foil	
C5	2.2 μF	electrolytic	63 V
C6	2.2 μF	electrolytic	63 V
C7	4.7 μF	electrolytic	63 V ±10%
C9	22 nF	foil	
C10	4.7 nF	foil	
C11	1 μF	electrolytic	63 V
C13	10 μF	electrolytic	63 V
C14	100 μF	electrolytic	16 V
C15	100 μF	electrolytic	16 V
R1	3.3 kΩ		
R2	15 kΩ		
R3	1.3 kΩ		
R4	100 kΩ		
Q1		CSB503F58	radial leads
		CSB503JF958	alternative as SMD

PINNING

SYMBOL	PIN	DESCRIPTION
SCL	1	serial clock input (I²C-bus)
V_{CC}	2	supply voltage
C_{PH}	3	capacitor for phase detector
CER	4	ceramic resonator
C_{P1}	5	capacitor for pilot detector
C_{P2}	6	capacitor for pilot detector
COMP	7	composite input signal
C_{MO}	8	capacitor DC-decoupling mono
C_{SS}	9	capacitor DC-decoupling stereo
R_{FR}	10	resistor for filter reference
n.c.	11	not connected
OUTL	12	output, left channel
OUTR	13	output, right channel
V_{ref}	14	reference voltage $0.5V_{CC}$
V_{CAP}	15	capacitor for electronic filtering of supply
C_{AV}	16	automatic volume control capacitor
TW	17	capacitor timing
C_W	18	capacitor for VCA and band-pass filter lower corner frequency
BPU	19	band-pass filter upper corner frequency
FDO	20	fixed de-emphasis output
FDI	21	fixed de-emphasis input
AGND	22	analog ground
DGND	23	digital ground
SDA	24	serial data input/output (I²C-bus)

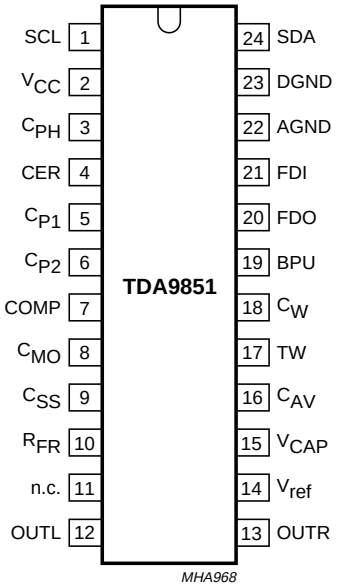


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Stereo decoder

The composite signal is fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 μs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded sub-signal L – R is sent to the VCA circuit. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator.

Mode selection

The L – R signal is fed via the internal VCA circuit to the dematrix/switching circuit. Mode selection is achieved via the I²C-bus.

Automatic volume level control

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range between 0.1 to 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and because of changes in the programme material. The function can be switched off. To avoid audible plops during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor (4.7 μF) at pin C_{AV} determines the attack and decay time constants. In addition the ratio of attack and decay times can be changed via the I²C-bus.

Integrated filters

The filter functions necessary for stereo demodulation are provided on-chip using transconductor circuits. The filter frequencies are controlled by the filter reference circuit via the external resistor R4.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	9.9	V
V_{SDA}, V_{SCL}	voltage of SDA and SCL to GND	V_{CC} < 9 V	0	V_{CC}	V
		V_{CC} ≥ 9 V	0	9	V
V_n	voltage of all other pins to GND		0	V_{CC}	V
T_{amb}	operating ambient temperature	T_j < 125 °C	–20	+70	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling	note 1	–	–	V

Note

1. Machine model class B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA9851 (SOT234-1; SDIP24)		55	K/W
	TDA9851T (SOT137-1; SO24)		90	K/W

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 9 V; R_s = 600 Ω; AC-coupled; R_L = 10 kΩ; C_L = 2.5 nF; f_{mod} = 1 kHz mono signal; composite input voltage 250 mV (RMS) for 100% modulation L + R (25 kHz deviation); T_{amb} = 25 °C; see Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		8	9	9.5	V
I_{CC}	supply current		–	30	40	mA
Input stage						
$V_{i(max)(rms)}$	maximum input voltage (RMS value)		2	–	–	V
Z_i	input impedance		20	25	30	kΩ
Stereo decoder						
HR	headroom for L + R, L and R	f_{mod} = 300 Hz; THD < 15%	9	–	–	dB
$V_{pil(rms)}$	nominal stereo pilot voltage (RMS value)		–	50	–	mV
$V_{th(on)(rms)}$	pilot threshold voltage stereo on (RMS value)		–	–	35	mV
$V_{th(off)(rms)}$	pilot threshold voltage stereo off (RMS value)		15	–	–	mV
hys	hysteresis		–	2.5	–	dB
$V_{o(rms)}$	output voltage (RMS value)	100% modulation L + R; f_{mod} = 300 Hz	–	500	–	mV
$\alpha_{csL,R}$	stereo channel separation L and R	14% modulation; f_L = 300 Hz; f_R = 3 kHz	–	20	–	dB
$THD_{L,R}$	total harmonic distortion L and R	100% modulation L or R; f_{mod} = 1 kHz	–	0.2	1.0	%
S/N	signal-to-noise ratio	mono mode; referenced to 500 mV output signal				
		CCIR 468-2 weighted; quasi peak	50	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA
Stereo decoder, oscillator (VCXO); note 1						
f_o	nominal VCXO output frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
Δf_{fr}	spread of free-running frequency	with nominal ceramic resonator	500.0	–	507.0	kHz
Δf_{cr}	capture range frequency	nominal pilot	±190	±265	–	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs OUTL and OUTR						
Z_o	output impedance		–	80	120	Ω
V_O	DC output voltage		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
R_L	output load resistance (AC-coupled)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
α_{ct}	crosstalk SAP into L and R	100% modulation; f_{mod} = 1 kHz; SAP; mode selector switched to stereo	50	70	–	dB
VCA						
I_s	nominal timing current for nominal release rate of VCA detector	I_s can be measured at pin TW via current meter connected to $0.5V_{CC}$ + 1 V	6.5	8	9.5	µA
Rel_{rate}	nominal detector release rate	nominal timing current and external capacitor values	–	125	–	dB/s
Automatic volume level control						
G_v	voltage gain	maximum boost; note 2	5	6	7	dB
		maximum attenuation; note 2	14	15	16	dB
G_{step}	equivalent step width between the input stages (soft switching system)		–	1.5	–	dB
$V_{iop(rms)}$	input voltage (RMS value)	maximum boost; note 2	–	0.1	–	V
		maximum attenuation; note 2	–	1.125	–	V
$V_{o(rms)}$	output voltage in AVL operation (RMS value)		160	200	250	mV
$V_{offset(DC)}$	DC offset voltage between different gain steps	voltage at pin C_{AV} 7.0 to 6.83 V or 6.83 to 6.61 V or 6.61 to 5.83 V or 5.83 to 3.1 V; note 3	–	–	20	mV
R_{att}	discharge resistors for attack time constant	AT1 = 0; AT2 = 0; note 4	340	420	520	Ω
		AT1 = 1; AT2 = 0; note 4	590	730	910	Ω
		AT1 = 0; AT2 = 1; note 4	0.96	1.2	1.5	kΩ
		AT1 = 1; AT2 = 1; note 4	1.7	2.1	2.6	kΩ
I_{dec}	charge current for decay time	normal mode; CCD = 0; note 5	1.6	2.0	2.4	µA
		power-**on** speed-up; CCD = 1; note 5	–	30	–	µA
Muting at power supply voltage drop for OUTR and OUTL						
ΔV_{CC}	supply voltage drop for mute active		–	V_{CAP} – 0.7	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-on reset; note 6						
$V_{POR(start)}$	start of reset voltage	increasing supply voltage	–	–	2.5	V
		decreasing supply voltage	4.2	5	5.8	V
$V_{POR(end)}$	end of reset voltage	increasing supply voltage	5.2	6	6.8	V
Digital part (I²C-bus pins); note 7						
V_{IH}	HIGH-level input voltage		3	–	$V_{CC} \leq 9$	V
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH-level input current		–10	–	+10	µA
I_{IL}	LOW-level input current		–10	–	+10	µA
V_{OL}	LOW-level output voltage	I_{IL} = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The oscillator is designed to operate together with Murata resonator CSB503F58 or CSB503JF958 as SMD. Change of the resonator supplier is possible, but the resonator specification must be close to the specified ones.
2. The AVL input voltage is internal. It corresponds to the output voltage OUTL and OUTR at AVL off.
3. The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, –6 dB and –15 dB.
4. Attack time constant = $C_{CAV} \times R_{att}$.
5. Decay time $= \dfrac{C_{CAV} \times 0.76\ V \left(10^{\frac{-G_1}{20}} - 10^{\frac{-G_2}{20}} \right)}{I_{dec}}$

   Example: C_{CAV} = 4.7 µF; I_{dec} = 2 µA; G_1 = –9 dB; G_2 = +6 dB → decay time results in 4.14 s.
6. When reset is active the GMU bit (mute) is set and the I²C-bus receiver is in the reset position.
7. The AC characteristics are in accordance with the I²C-bus specification for standard mode (clock frequency maximum 100 kHz). A higher frequency, up to 280 kHz, can be used if all clock and data times are interpolated between standard mode (100 kHz) and fast mode (400 kHz) in accordance with the I²C-bus specification. Information about the I²C-bus can be found in brochure *"I²C-bus and how to use it"* (order number 9398 393 40011).

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	DATA	P

Table 1 Explanation of I²C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition; generated by the master
Standard SLAVE ADDRESS (MAD)	101 101 1
R/$\overline{W}$	logic 1 (read); generated by the master
A	acknowledge; generated by the slave
DATA	slave transmits an 8-bit data word
P	STOP condition; generated by the master

Table 2 Definition of the transmitted bytes after read condition

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Y	Y	Y	Y	Y	Y	Y	STP

Table 3 Function of the bits in Table 2

BITS	FUNCTION
STP	stereo pilot identification (stereo received = 1)
Y	indefinite

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	DATA	A	P

Table 4 Explanation of I²C-bus format to write (slave receives data)

NAME	DESCRIPTION
S	START condition
Standard SLAVE ADDRESS (MAD)	101 101 1
R/$\overline{W}$	logic 0 (write)
A	acknowledge; generated by the slave
DATA	see Table 5
P	STOP condition

Table 5 Definition of the DATA (second byte after MAD)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	AT2	AT1	CCD	AVLON	GMU	STEREO

Table 6 Function of the bits in Table 5

BITS	FUNCTION
STEREO	mode selection stereo or mono
GMU	mute control OUTL and OUTR
AVLON	AVL **on/off**
CCD	increased AVL decay current **on/off**
AT1 and AT2	attack time at AVL

Table 7 Mode setting

FUNCTION MODE		READABLE BIT STP	SETTING BIT STEREO
OUTL	OUTR		
Left	right	1 (stereo received)	1
Mono	mono	1 (stereo received)	0
Mono	mono	0 (no stereo received)	1
Mono	mono	0 (no stereo received)	0

Table 8 Mute setting

FUNCTION	DATA GMU
Forced mute at OUTR and OUTL	1
No forced mute at OUTR and OUTL	0

Table 9 AVLON bit setting

FUNCTION	DATA
Automatic volume control **on**	1
Automatic volume control **off**	0

Table 10 CCD bit setting

FUNCTION	DATA
Load current for normal AVL decay time	0
Increased load current	1

Table 11 AVL attack time

R_{att} (Ω)	DATA	
	AT1	AT2
420	0	0
730	1	0
1200	0	1
2100	1	1

INTERNAL PIN CONFIGURATIONS

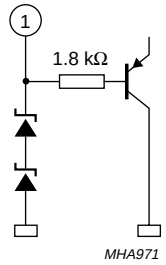


Fig.3 Pin 1; SCL.

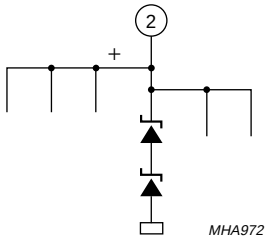


Fig.4 Pin 2; V_{CC}.

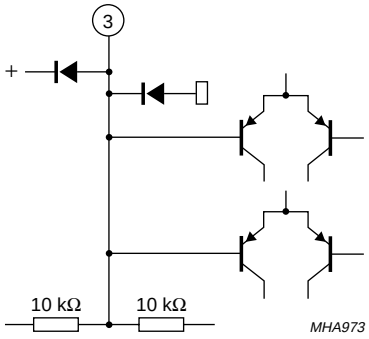


Fig.5 Pin 3; C_{PH}.

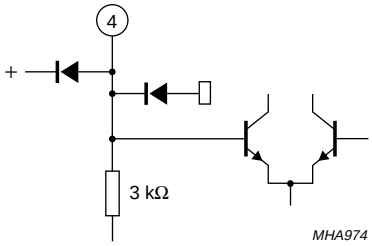


Fig.6 Pin 4; CER.

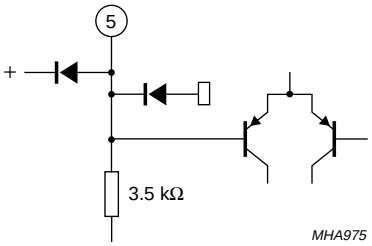


Fig.7 Pin 5; C_{P1}.

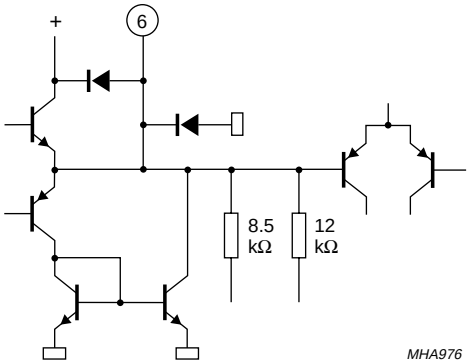


Fig.8 Pin 6; C_{P2}.

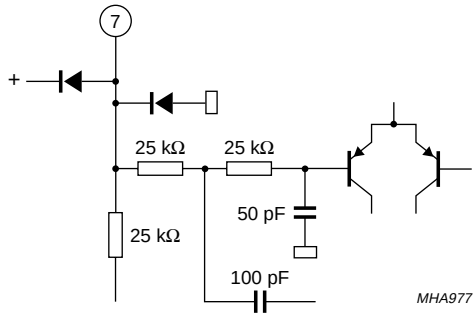


Fig.9 Pin 7; COMP.

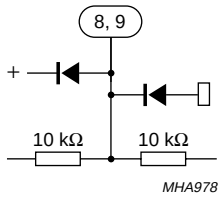


Fig.10 Pin 8; C_{MO} and pin 9; C_{SS}.

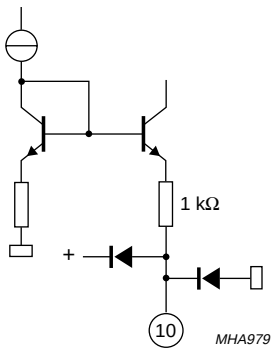


Fig.11 Pin 10; R_{FR}.

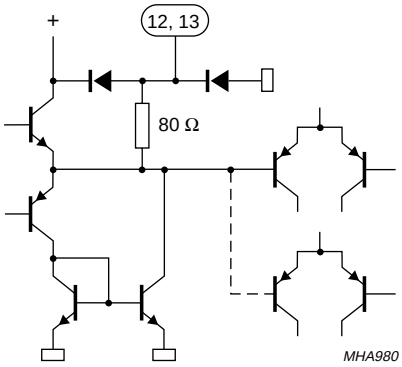


Fig.12 Pin 12; OUTL and pin 13; OUTR.

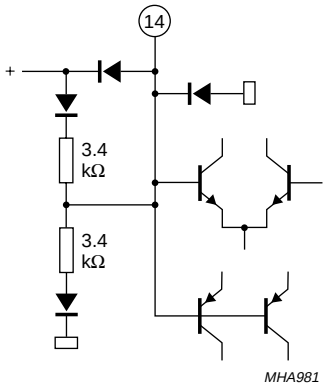


Fig.13 Pin 14; V_{ref}.

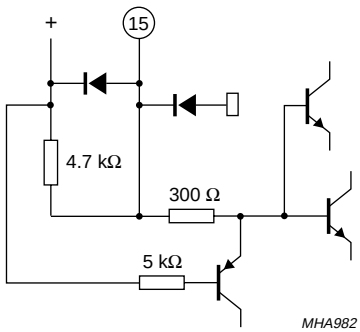


Fig.14 Pin 15; V_{CAP}.

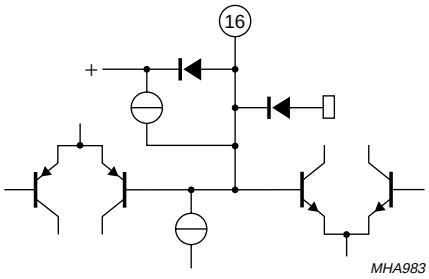


Fig.15 Pin 16; C_{AV}.

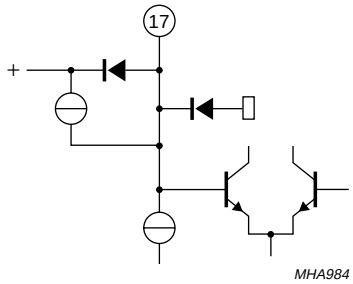


Fig.16 Pin 17; TW.

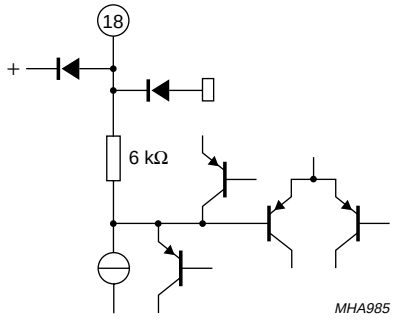


Fig.17 Pin 18; C_W.

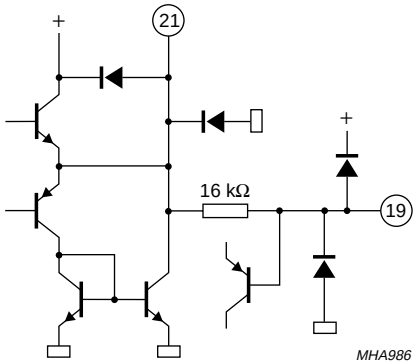


Fig.18 Pin 19; BPU and pin 21; FDI.

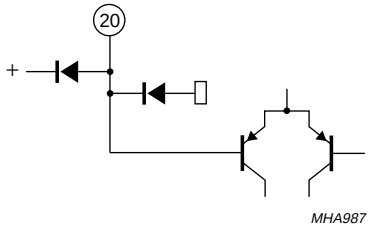


Fig.19 Pin 20; FDO.

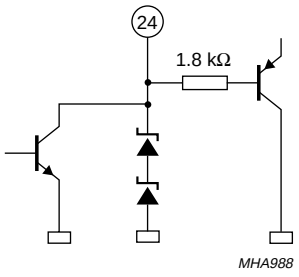


Fig.20 Pin 24; SDA.

APPLICATION INFORMATION

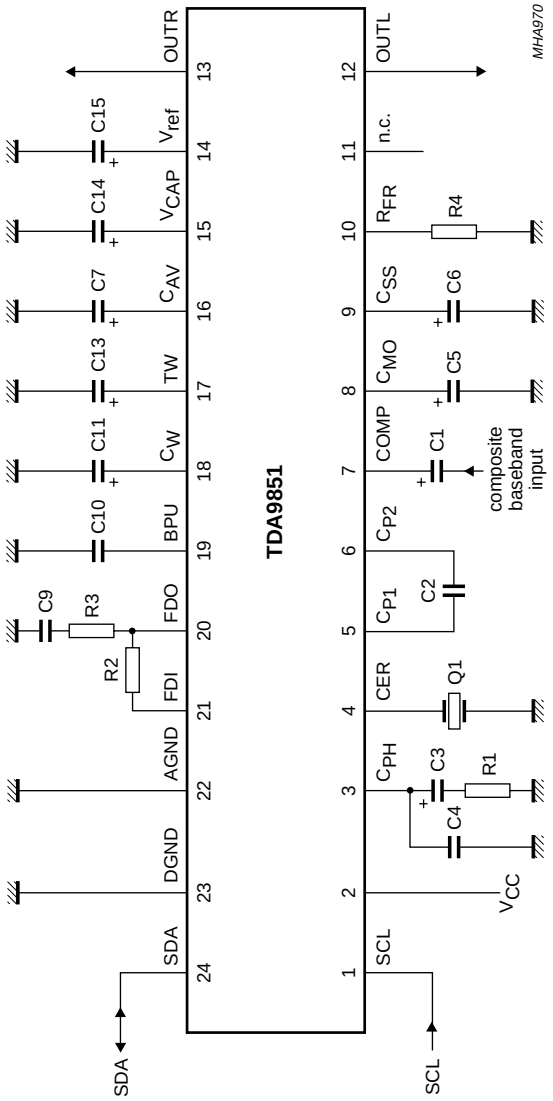
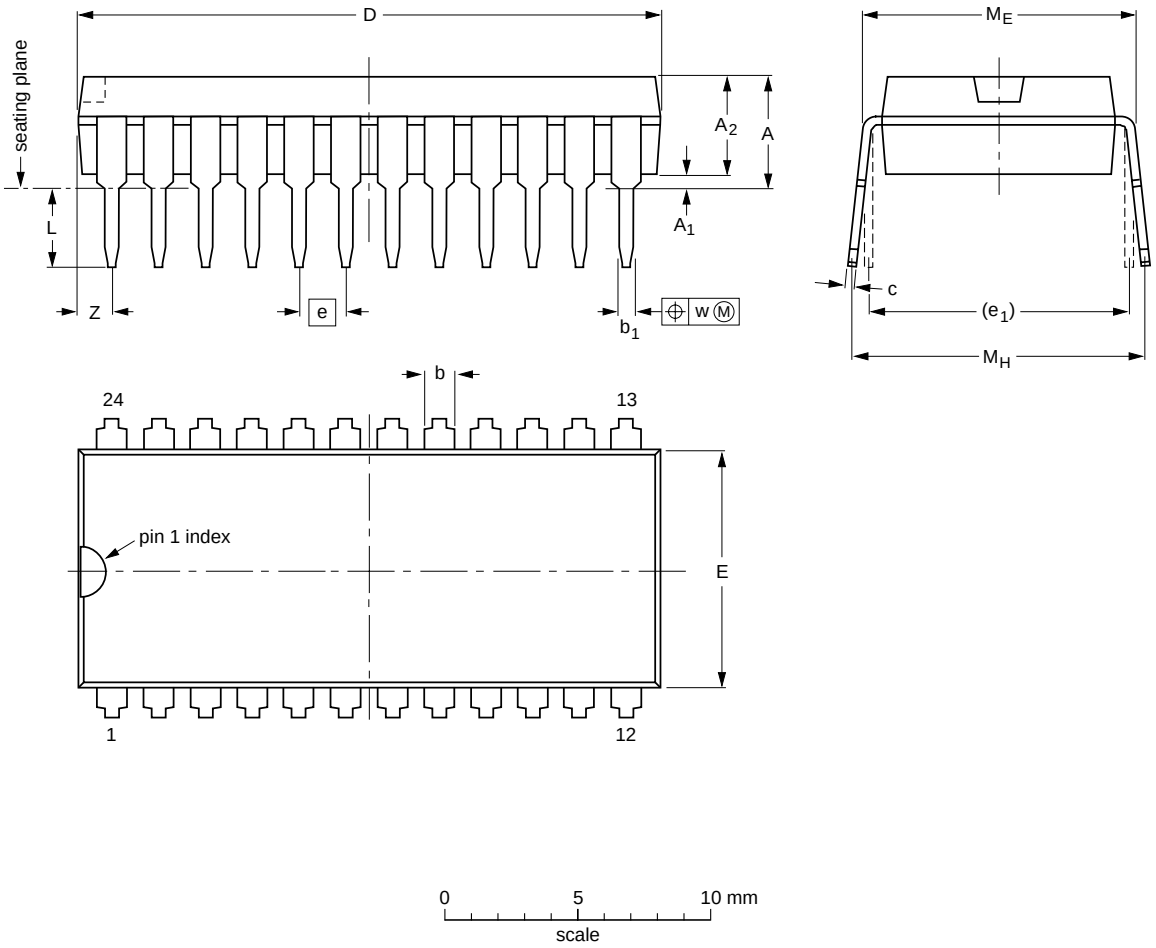


Fig.21 Application circuit.

PACKAGE OUTLINES

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

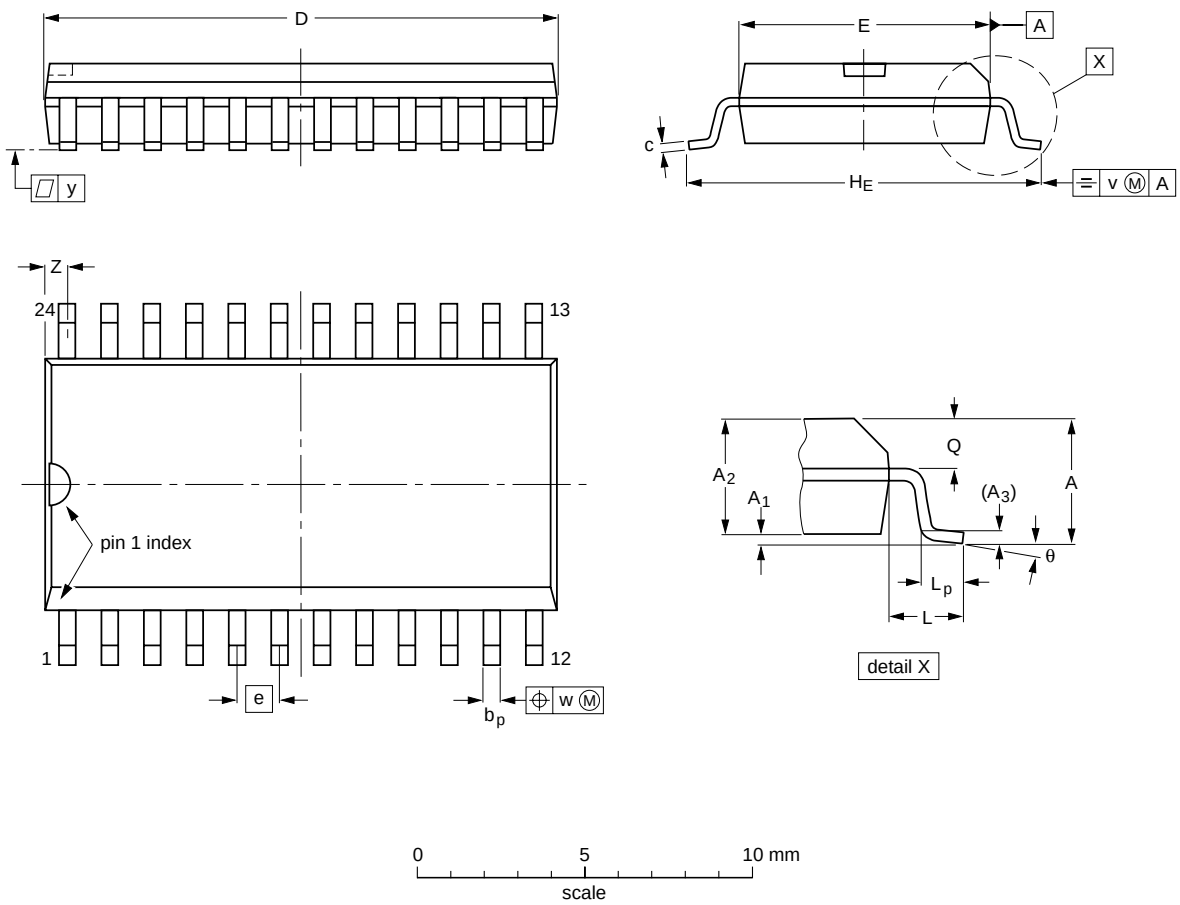
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

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	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

SDIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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